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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,805	03/26/2004	GENG-LIN CHEN	12264-US-PA	2804

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
06/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/708,805	CHEN ET AL.	
	Examiner	Art Unit	
	Ryan M. Stiglic	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending and have been examined.

2. Claims 1-19 are rejected.

Response to Arguments

3. Applicant's arguments filed March 21, 2007 have been fully considered but they are not persuasive. In their arguments dated March 21, 2007 applicant states, "In rejecting claim 1, the Examiner interpreted item 28a as a shared bus. However, Greeff teaches: "[T]he processor system 20 ... connected to a memory controller 31 with "a segmented data bus 28" (including bus segments 28a, 28b, and 28c) (Paragraph [0031] and Fig. 1). **Applicants believe that if item 28a is interpreted as a shared bus, then the others, i.e., 28b, 28c, which are identical to item 28a, should also be interpreted in such a manner as shared buses, and therefore Greeff teaches more than one shared bus which is critical for his processor system 20, rather than a single shared bus (Emphasis added)**." The Examiner respectfully disagrees. Figure 1 of Greeff shows a two-device system (namely first device 24 and second device 26). Applicant's belief that items 28a and 28b are identical and that both 28a and 28b should be interpreted as shared buses is not accurate. The Examiner's interpretation of item 28a being equivalent to applicant's single shared bus stems from not only the devices connected to 28a but also the traffic carried over 28a. Single shared bus 28a (Greeff; Fig. 1) connects control apparatus 31 and first device 24 and thus transfers data to/from first device 24. Single shared bus 28a also transfer data to/from device 26 in that when control apparatus 31 sends/receives data to/from device 26 the data must pass through single shared bus 28a. In their two-device system of Figure 1, Greeff

discloses the bus segment 28b only transfers data to/from device 26. Therefore the bus segment 28b cannot be interpreted as a shared bus as applicant contends it should be. For these reasons, applicant's arguments are not persuasive and the previous grounds of rejection are maintained.

4. Regarding applicant's arguments relating to the rejection of claims 2-3 and 7-11 under 35 U.S.C. § 103(a), the Examiner is not persuaded. Applicant contends "In rejecting claim 2, the Examiner has apparently neglected above required procedures (B), (C), and (D)" (referring to the factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966)) and "[T]here is no modification or combination proposed at all, and there is certainly no explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the inexistent proposed modification". As noted by the applicant, "[T]here is no modification or combination proposed at all," instead the Examiner is relying upon the *teachings* of Greeff as a whole to show that an artisan would find the subject matter claimed to be obvious in view of Greeff. Moreover, applicant argues, "The Examiner is more likely using his own knowledge or common knowledge to crossover the gap between the claimed invention and Greeff". "Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it." *KSR International Co. v. Teleflex, Inc. Supreme Court Decision No. 04-1350.*

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1,4-6, 12-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Greeff et al. (US Patent Application Publication No. 2002/0083255).

For claim 1 Greeff discloses:

A system for accessing at least a first device (Fig. 1+, item 24) and a second device (Fig. 1+, item 26), the system comprising:

- a single shared bus, coupled to the first device (Fig. 1+, item 28a);
- a bus isolator (Fig. 2, item 39), coupled to the shared bus and the second device for isolating the second device from the single shared bus or connecting the second device to the single shared bus ([0036]); and
- a control apparatus (Fig. 1+, item 31) coupled to the single shared bus so that the bus isolator isolates the second device from the single shared bus when the control apparatus needs to access the first device and the bus isolator connects the second device with the single shared bus when the control apparatus needs to access the second device ([0036; 0040-0044]).

For claim 4 Greeff discloses:

The system of claim 1, wherein the second device comprises a memory card compatible device (The memory devices may be printed on printed circuit boards thus representing a memory card [0052]).

For claims 5 and 14 Greeff discloses:

The system of claim 4, wherein the memory card compatible device is either a memory card (The memory devices may be printed on printed circuit boards thus representing a memory card [0052]) or a card reader.

For claim 6 Greeff discloses:

The system of claim 1, wherein the first device comprises a memory device ([0031])

For claim 12 Greeff discloses:

A system using a single bus for accessing a plurality of devices, comprising:

- a memory unit (Fig. 1+, item 24; [0031]);
- a memory card compatible device (Fig. 1+, item 26; [0031,0052]);
- a shared bus (Fig. 1+, item 28a), coupled to the memory unit; and
- a control apparatus (Fig. 1+, item 31) coupled to the shared bus such that the control apparatus controls the shared bus to connect with a circuit internally linked to the memory unit when the control apparatus needs to access the memory unit and the control apparatus controls the shared bus to connect with a circuit internally linked to the

memory card compatible device when the control apparatus needs to access the memory card compatible device ([0036; 0040-0044]).

For claim 13 Greeff discloses:

The system of claim 12, wherein a pre-defined isolation period must pass before the control apparatus is permitted to access the second device through the shared bus (The invention of Greeff relates to switches that "are configured to connect those segments required for communication between currently select data input/output devices, e.g. memory modules, and disconnecting the remaining segments [0009]." Therefore in order for a second device to transfer data across the shared bus it must wait for the "pre-defined isolation period" [referring to the period of time the second device is isolated while a first device is transmitting data] to expire before it transmits its data.)

For claim 15 Greeff discloses:

The system of claim 12, wherein the memory unit comprises read-only memory ([0072]).

For claim 16 Greeff discloses:

A system using a single bus for accessing a plurality of devices, comprising:

- a first device (Fig. 1+, item 24);
- a second device (Fig. 1+, item 26);
- a shared bus, coupled to the first device (Fig. 1+, item 28a);

- a bus isolator (Fig. 2, item 39), coupled to the shared bus and the second device for isolating the second device from the shared bus or connecting the second device to the shared bus ([0036]); and
- a control apparatus (Fig. 1+, item 31) coupled to the shared bus so that the bus isolator isolates the second device from the shared bus when the control apparatus needs to access the first device and the bus isolator connects the second device with the shared bus when the control apparatus needs to access the second device, wherein the bus isolator is controlled by the control apparatus to isolate the first device and the second device from the shared bus in consideration of signaling demand for data transmission to prevent any data error resulting from a mutual interference of the signal transmission between the first device and the second device ([0036; 0040-0044]; Likewise Greeff discloses the ability to use isolation devices to completely isolate all devices not required for communication (see figures 12-15 and 17 where bus isolator isolate the components of a first/second device from the bus simply connect the bus segments to create a true point-to-point bus [0062-0069]).

For claim 17 Greeff discloses:

The system of claim 16, wherein a triggering signal is transmitted to the bus isolator for performing the isolation ([0050]).

For claim 19 Greeff discloses:

The system of claim 16, wherein a pre-defined isolation period is expired when the bus exchanger is permitted to switch the first device of the second device for authority for the shared bus (The invention of Greeff relates to switches that "are configured to connect those segments required for communication between currently select data input/output devices, e.g. memory modules, and disconnecting the remaining segments [0009]." Therefore in order for a second device to transfer data across the shared bus it must wait for the "pre-defined isolation period" [referring to the period of time the second device is isolated while a first device is transmitting data] to expire before it transmits its data.).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3 and 7-11 rejected under 35 U.S.C. 103(a) as being unpatentable over Greeff et al. (US Patent Application Publication No. 2002/0083255).

For claim 2 Greeff teaches:

The system of claim 1, wherein the control apparatus further comprises:

- a bus exchanger, coupled to the single shared bus for switching the authority for the single shared bus between different devices (The memory controller 31 must include an

interface [shown generally as 30] that passes the signals from the controller to the I/O or memory devices. "Each integrated interface circuit 30 permits data exchange between the segmented data bus 28 and another pathway [0031]." Therefore, since the interface 30 of the memory controller 31 must pass the "memory system command and address bus 135 [0043]" to the I/O or memory devices 24/26 the limitation of a bus exchanger, coupled to the shared bus for switching the authority for the shared bus between different devices is functionally equivalent to the interface 30 of the memory controller 31.); and

- a bus arbitrator, coupled to the bus exchanger so that the bus arbitrator controls the bus exchanger to connect the single shared bus with a circuit internally linked to the first device when the control apparatus needs to access the first device and the bus arbitrator controls the bus exchanger to connect the single shared bus with a circuit internally linked to the second device when the control apparatus needs to access the second device (While not explicitly disclosed in the specification/drawings of Greeff, the memory controller 31 inherently comprises internal circuit necessary to initiate a WRITE or READ [0053] across the shared bus 28. As part of a transaction across the bus 28 the memory controller *must* control the operation of isolation devices 39 in order to facilitate data transfer to a destination device 24/26 [0043]. Therefore the internal circuitry of the memory controller 31 is functionally equivalent to the bus arbitrator of the instant application because the internal circuitry of the memory controller instructs the interface device to transmit control signals to devices in order to facilitate data movement.).

For claims 3 and 8 Greeff teaches:

The system of claim 2, wherein a pre-defined isolation period must pass before the bus exchanger is permitted to switch the device for authority for the single shared bus (The invention of Greeff relates to switches that "are configured to connect those segments required for communication between currently select data input/output devices, e.g. memory modules, and disconnecting the remaining segments [0009]." Therefore in order for a second device to transfer data across the shared bus it must wait for the "pre-defined isolation period" [referring to the period of time the second device is isolated while a first device is transmitting data] to expire before it transmits its data.).

For claim 7 Greeff teaches:

A control apparatus (Fig. 1+, item 31) for accessing a plurality of devices (Fig. 1+, items 24/26) through a single bus (Fig. 1+, item 28), the control apparatus connects to a first device through a shared bus (Fig. 1+, item 28a) and the control apparatus also connects to a second device through the shared bus and a bus isolator (Fig. 2, item 39; [0036]), the control apparatus comprising :

- a bus exchanger, coupled to the shared bus for switching the authority of device for the shared bus (The memory controller 31 must include an interface [shown generally as 30] that passes the signals from the controller to the I/O or memory devices. "Each integrated interface circuit 30 permits data exchange between the segmented data bus 28 and another pathway [0031]." Therefore, since the interface 30 of the memory controller 31 must pass the "memory system command and address bus 135 [0043]" to the I/O or memory devices 24/26 the limitation of a bus exchanger, coupled to the shared bus for

switching the authority for the shared bus between different devices is functionally equivalent to the interface 30 of the memory controller 31.); and

- a bus arbitrator coupled to the bus exchanger such that the bus arbitrator controls the bus exchanger to connect with a circuit internally linked to the first device and to activate the bus isolator to isolate the second device from the shared bus when the control apparatus needs to access the first device and the bus arbitrator controls the bus exchanger to connect with a circuit internally linked related to the second device when the control apparatus needs to access the first device (While not explicitly disclosed in the specification/drawings of Greeff, the memory controller 31 inherently comprises internal circuit necessary to initiate a WRITE or READ [0053] across the shared bus 28. As part of a transaction across the bus 28 the memory controller *must* control the operation of isolation devices 39 in order to facilitate data transfer to a destination device 24/26 [0043]. Therefore the internal circuitry of the memory controller 31 is functionally equivalent to the bus arbitrator of the instant application because the internal circuitry of the memory controller instructs the interface device to transmit control signals to devices in order to facilitate data movement.).

For claim 9 Greeff teaches:

The control apparatus of claim 7, wherein the second device comprises a memory card compatible device (The memory devices may be printed on printed circuit boards thus representing a memory card [0052]).

For claim 10 Greeff teaches:

The control apparatus of claim 7, wherein the memory card compatible device is either a memory card (The memory devices may be printed on printed circuit boards thus representing a memory card [0052]) or a card reader.

For claim 11 Greeff teaches:

The control apparatus of claim 7, wherein the first device comprises a memory unit ([0031]).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greeff et al. as applied to claim 17 above, and further in view of Chao (US Patent No. 7,099,972).

As noted above, Greeff discloses a system for accessing a plurality of devices using a single bus, comprising:

- a first device (Fig. 1+, item 24);
- a second device (Fig. 1+, item 26);
- a shared bus, coupled to the first device (Fig. 1+, item 28a);
- a bus isolator (Fig. 2, item 39), coupled to the shared bus and the second device for isolating the second device from the shared bus or connecting the second device to the shared bus ([0036]); and
- a control apparatus (Fig. 1+, item 31) coupled to the shared bus so that the bus isolator isolates the second device from the shared bus when the control apparatus needs to access the first device and the bus isolator connects the second device with the shared bus when

the control apparatus needs to access the second device, wherein the bus isolator is controlled by the control apparatus to isolate the first device and the second device from the shared bus in consideration of signaling demand for data transmission to prevent any data error resulting from a mutual interference of the signal transmission between the first device and the second device ([0036; 0040-0044]; Likewise Greeff discloses the ability to use isolation devices to completely isolate all devices not required for communication (see figures 12-15 and 17 where bus isolator isolate the components of a first/second device from the bus simply connect the bus segments to create a true point-to-point bus [0062-0069]).

While Greeff discloses a system and method for eliminating bus reflections and improving data rates they do not disclose a means for arbitrating for requests of data transfers among competing resources.

Chao discloses a system and method for arbitrating access to a system resource (i.e. the shared bus of Greeff) such that requests for transfer from devices with lower demand are granted first (col. 2, ll. 18-41). By granting access to the shared bus based on lower demand idle time between requests is substantially reduce (col. 1, ll. 52-58).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to connect the bus device with the lowest demand, as per the teachings of Chao, prior to connecting (granting) the device with the higher demand such that idle times between requests

is reduced. Reducing idle time increases data rate thus providing a greater improvement to the system of Greeff which also increases data rate.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RMS

PAUL R. MYERS
PRIMARY EXAMINER